26. A semiconductor memory chip according to claim 1, further including means defining a read cycle and a write cycle, each comprising a fixed plurality of the clock pulses including the series of clock pulses, with a first clock pulse of the read cycle and a first clock pulse of the write cycle corresponding to the firstly occurred clock pulse of the series of clock pulses.

27. A semiconductor memory chip according to claim 26, wherein a last clock pulse of the read cycle and a last clock pulse of the write cycle correspond to a last clock pulse of the series of clock pulses.

28. A semiconductor memory chip according to claim 27, wherein each of the read cycle and the write cycle have a second clock pulse corresponding to the subsequent clock pulse, and a third clock pulse corresponding to the last clock pulse and defining a pre-charge period.

29. A semiconductor memory chip according to claim 1, wherein said means for generating generates the row address set signal and the column address set signal in responsive to only the clock signal and further is enabled by at least said chip select signal.

30. A semiconductor memory chip according to claim 1, wherein said first mentioned means for setting includes a row latch inputting the row address set signal and the address signal and outputting the row address signal;

said second mentioned means for setting including a column latch inputting the column address set signal and the address signal, and outputting the column address signal.

31. A semiconductor RAM chip of claim 4, wherein said means for receiving and outputting includes a row latch inputting the address signal and outputting the row address, and a column latch outputting the column address.

32. A semiconductor RAM chip of claim 4, wherein said means for receiving and for outputting generates the row address at a timing responsive to an edge of the clock pulses and is enabled by the chip select signal.

33. The semiconductor RAM of claim 4, wherein said means for receiving and for outputting is enabled by the chip select signal and demultiplexes the address signal in response to the timing of the clock pulses.

34. The semiconductor RAM of claim 33, wherein said means for receiving and for outputting has inputs of only the clock, the chip select signal and the address signal.

35. The semiconductor memory of claim 15, wherein said demultiplexing means has inputs of only the clock, the address signal, and the control signal.

36. The semiconductor memory of claim 15, wherein said demultiplexing means is enabled by only the control signal.

37. The semiconductor memory of claim 15, wherein said demultiplexing means includes a control circuit consisting of logic elements, including a logic element having an edge trigger directly connected to the clock input terminal.

38. The semiconductor memory of claim 15, wherein said demultiplexing means includes a row latch inputting a row address set signal and the address signal, and outputting the row addresses to the row address decoder; and

said demultiplexing means further including a column latch inputting a column address set signal and the address signal, and outputting the column addresses to the column address decoder.

39. The semiconductor memory of claim 38, wherein said demultiplexing means further includes a control circuit inputting the clock and the control signal, and outputting the column address set signal and the row address set signal respectively to the column latch and the row latch.

40. A dynamic random access memory (DRAM), comprising:

a clock input for receiving a clock having a periodic succession of clock pulses;

a dynamic random access memory cell array;

a data output connected to said memory cell array to output data from said memory cell array;

a row address decoder having a row address input and an output connected to said memory cell array;

a column address decoder having a column address input and an output connected to said memory cell array; and

a demultiplexer for receiving an address signal having row addresses and column addresses time multiplexed, for demultiplexing the address signal in response to timing of the clock pulses of the clock, for outputting the row addresses to the row address input of the row address decoder separate from the column addresses, and for outputting the column addresses to the column address input of the column address decoder separate from the row address.

41. A memory according to claim 40, wherein said demultiplexer includes a row latch inputting a row address set signal and the address signal, and outputting the row addresses to the row address decoder; and

said demultiplexer further including a column latch inputting a column address set signal and the address signal, and outputting the column addresses to the column address decoder.

42. A memory according to claim 41, wherein said demultiplexer further includes a control circuit inputting the clock and a control signal, and outputting the column address set signal and the row address set signal respectively to the column latch and the row latch.

43. A dynamic random access memory chip, comprising:

a dynamic random access memory cell array;

a row select circuit for receiving a row address signal and setting a row address in the memory cell array;

a column select circuit for receiving a column address signal and setting a column address in the memory cell array; and

a page mode select circuit setting a plurality of sequential column addresses in the memory cell array while holding the setting of the row address without changing the row address and determining the timing of setting the column addresses only in accordance with timing of an external clock.

44. The memory chip according to claim 43, wherein each of said column select circuit, said row select circuit and said page mode select circuit are enabled by one or more external control signals.

45. The memory chip according to claim 44, wherein each of said column select circuit and said row select circuit set the column address and the row address at a timing determined by the external clock.

46. The memory chip according to claim 45, wherein said row select circuit and said column select circuit comprise a demultiplexer for commonly receiving a single address signal containing column and row addresses time multiplexed.

47. A semiconductor dynamic random access memory chip, comprising:

a dynamic random access memory cell array;

means for receiving address signals having a row address signal and a column address signal;

means for receiving an external clock signal having a single periodic succession of clock pulses;

means for receiving a chip select signal;

a data output terminal coupled to said dynamic random access memory cell array for outputting data;

a data input terminal coupled to said dynamic random access memory cell array for receiving data;

means for inputting said external clock signal and said chip select signal and for generating a row address set signal and a column address set signal;

a row address latch for latching the row address signal in response to the row address set signal;

a column address latch for latching the column address signal in response to the column address set signal;

a row address decoder coupled between said dynamic random access memory cell array and said row address latch;

a column address decoder coupled between said dynamic random access memory cell array and said column address latch;

first latch means coupled between said data output terminal and said dynamic random access memory cell array for latching the data from said dynamic random access memory cell array in synchronism with said external clock signal; and

second latch means coupled between said data input terminal and said dynamic random access memory cell array for latching the data to said dynamic random access memory cell array in synchronism with said external clock signal.

48. A semiconductor dynamic random access memory chip according to claim 47, wherein the address signals having the row address signals and the column address signals are time multiplexed; and said means for generating, row address latch and column address latch comprise a demultiplexer for demultiplexing the address signals.

49. A system, comprising:

a computer system producing a system clock with a single periodic succession of clock pulses; and

a semiconductor dynamic random access memory chip, comprising

a dynamic random access memory cell array,

an address input terminal for receiving address signals having a row address signal and a column address signal,

a clock input terminal for receiving the system clock,

a data output terminal coupled to said dynamic random access memory cell array for outputting data,

a data input terminal coupled to said dynamic random access memory cell array for receiving data,

a chip select input terminal for receiving a chip select signal,

a control circuit for inputting the system clock and the chip select signal, and for generating a row address set signal and a column address set signal,

a row address latch for receiving the address signals and latching the row address signal in response to the row address set signal,

a column address latch for receiving the address signals and latching the column address signal in response to the column address set signal,

a row address decoder coupled between said dynamic random access memory cell array and said row address latch,

a column address decoder coupled between said dynamic random access memory cell array and said column address latch,

a first latch coupled between said data output terminal and said dynamic random access memory cell array for latching the data from said dynamic random access memory cell array in synchronism with the system clock, and

a second latch coupled between said data input terminal and said dynamic random access memory cell array for latching the data to said dynamic random access memory cell array in synchronism with the system clock.

50. A semiconductor dynamic random access memory chip according to claim 49, wherein the address signals having the row address signals and the column address signals are time multiplexed; and said means for generating, row address latch and column address latch comprise a demultiplexer for demultiplexing the address signals.